CSE369 Practice Problems (lec 6)

1. More FSMs

1.1] Draw the state diagram that recognize the bit string "101" with the following behavior:

```
Input:     1 0 0 1 0 1 0 1 1 0 0 1 0
Output:    0 0 0 0 0 1 0 1 0 0 0 0 0
```

1.2] How many cycles would we need to **fully** test this FSM from reset?

1.3] Draw a **truth table** for your state diagram. The inputs to the truth table should be the two bits of the present state **PS[1:0]** and the one bits of the FSM input, **IN**. The outputs should be the two next state bits **NS[1:0]** and the output **Out**.

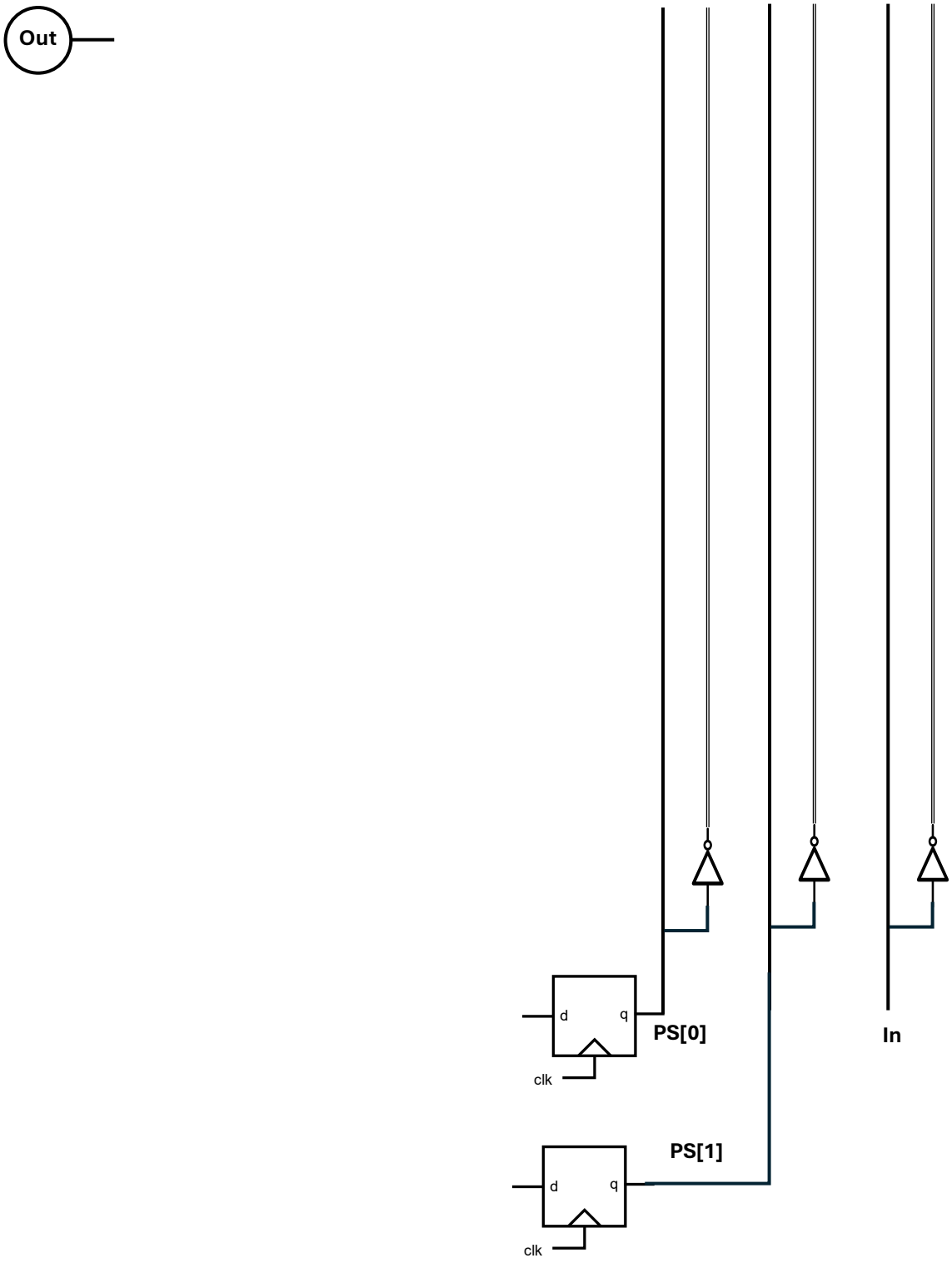
1.4] When you're done with the truth table, solve a k-map for each of the three output bits and use it to make a minimal two-level Boolean equation. Write that equation here:

NS[0] =

NS[1] =

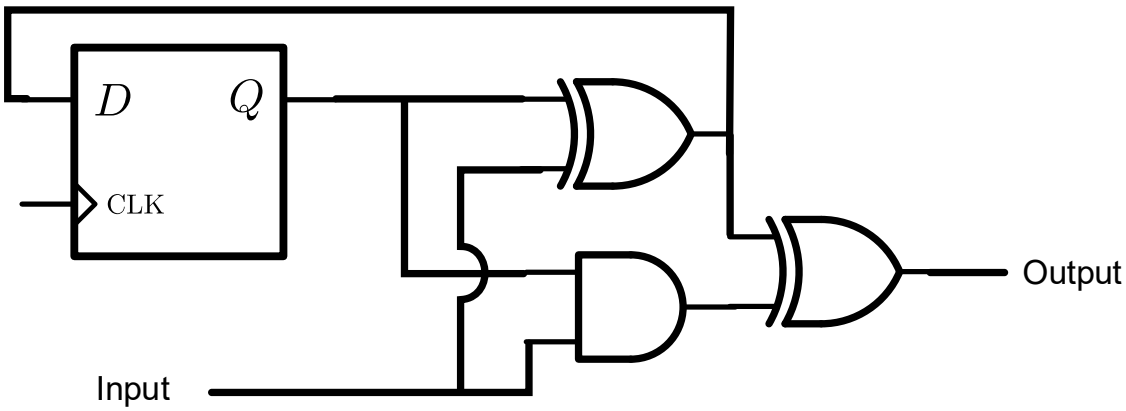
Out =

1.5] Draw gates on the diagram below to complete your FSM design:



2. Timing Constraints

Consider the following circuit with t_{AND} = **6 ns** and t_{XOR} = **9 ns**. Assume the input changes consistently at t_{input} = **2 ns** after the rising edge of the clock, and that there are no timing requirements for the Output port.



2.1] Assume t_{setup} = **4 ns**, t_{hold} = **10 ns** and t_{period} = **20 ns**. What is the minimum and maximum t_{C2Q} this circuit can support?

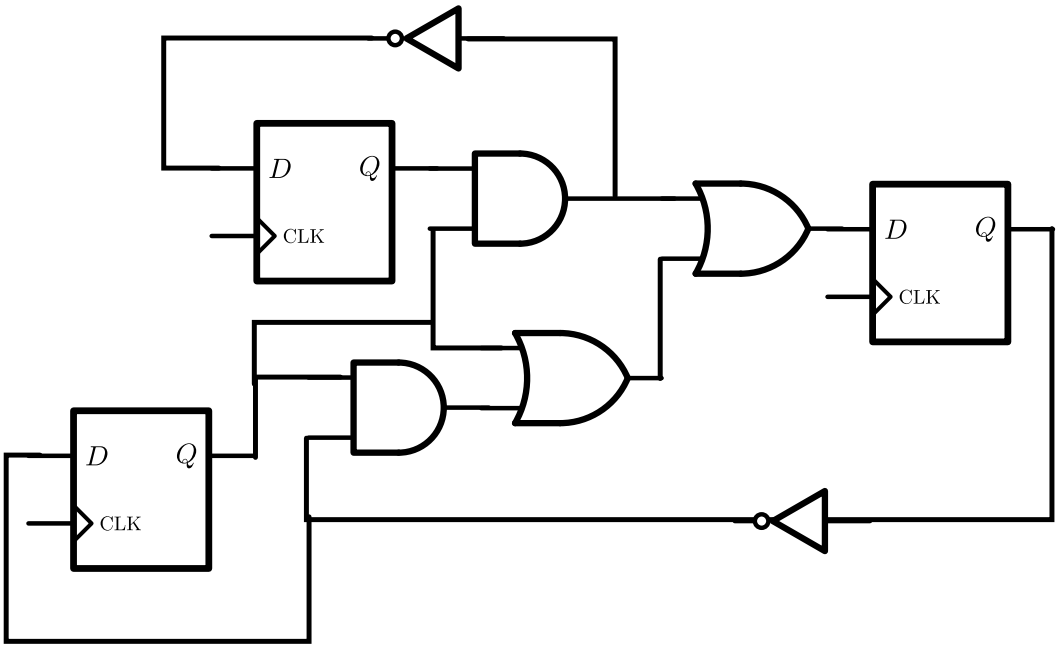
2.2] Assume t_{C2Q} = **3 ns** and t_{period} = **20 ns**. What is the maximum t_{setup} this circuit can tolerate? What is the minimum t_{hold} this circuit can tolerate?

2.3] Now assume t_{C2Q} = **3 ns,** t_{Input} = **10 ns** and t_{period} = **20 ns**. What is the maximum t_{setup} this circuit can tolerate?

2.4] Assume t_{C2Q} = t_{setup} = t_{input} = **2 ns**. What is the minimum t_{period} this circuit can tolerate?

3. More Timing Constraints

Consider the following circuit, assuming all gates and C2Q delay are 1 ns:



On the diagram above, highlight the critical path. In another color, highlight the min-path.